REMARKS

In response to the final Office Action of November 1, 2007, applicant asks that all claims be allowed in view of the amendments to the claims and the following remarks.

Claims 1, 7, 18, 20, 21, 28, 59, 60, 63-66, and 71-87 are now pending, of which claims 1, 18, 20, 76, and 82 are independent. Claims 1, 18, 20, 21, 28, and 59 have been amended; claims 2-6, 8-17, 19, 22-27, 61, 62, and 67-70 have been cancelled; and claims 71-87 have been added. Support for the amendments and new claims may be found in the originally filed application at, for example, page 7, lines 22-26; page 15, line 25 to page 17, line 7; and FIGS. 1 and 16. No new matter has been added.

This response is being filed concurrently with a Request for Continued Examination.

Claim Objections

The Examiner has objected to claims 10 and 18 have been objected to, and the amendments to claims 10 and 18 are believed to address the Examiner's concerns. Accordingly, applicant requests reconsideration and withdrawal of the objections.

Claim Rejections—35 U.S.C. § 103

Claims 1, 7, and 64

Claims 1, 7, and 64 have been rejected as being unpatentable over U.S. Patent No. 6,373,454 (Knapp) in view of JP 2001-296873 (Noboru).[1] Applicant requests reconsideration and withdrawal of this rejection because neither Knapp, Noboru, nor any proper combination of these references describes or suggests the subject matter of amended claim 1.

Among other features, amended claim 1 recites a driven circuit including a first transistor, a signal line electrically connected to the first transistor through a node, and a first precharge circuit electrically connected to the signal line and including a second transistor, where a gate width of the second transistor is larger than a gate width of the first transistor. Neither

[1] The Office Action refers to JP 2001-296873 as Noboru, thus the applicant also refers to this reference as Noboru. However, applicant notes that Noboru is a first name and the family name of the inventor is Asahi.

Knapp, Noboru, nor any proper combination of these references describes or suggests these features.

In Knapp, a panel includes electroluminescent display elements 20 located at intersections between row and column address conductors 12 and 14, and each display element 20 has an associated switch that is connected to the row and column conductors 12 and 14. See Knapp at col. 5, lines 24-30 and 42-46; col. 6, lines 6-8. The switch includes an n-channel field effect transistor 30 with a drain terminal connected through a switch 33 to the cathode of the display element 20. See Knapp at col. 6, lines 21-26. The gate of the transistor 30 is connected through a switch 32 to the drain of the transistor 30. See Knapp at col. 6, lines 32-34. An input line 35 connects to a node 36 between the switches 32 and 33 though a switch 37. See Knapp at col. 6, lines 39-43. The switches 32, 33, and 37 may be a formed as thin film field effect transistors. See Knapp at col. 7, lines 28-32.

The Office Action equates the transistor 30 with the recited first transistor. See Office Action at page 2, line 19. However, even assuming that the transistor 30 may be equated with the recited first transistor, there is no indication that any of Knapps' other transistors 32, 33, and 37 have a gate width larger than a gate width of transistor 30. Thus, Knapp does not describe or suggest a driven circuit including a first transistor, and a first precharge circuit electrically connected to a signal line and including a second transistor, where a gate width of the second transistor is larger than a gate width of the first transistor, as recited in amended claim 1.

Noboru, which is cited as showing "a precharge voltage is supplied to the node through the signal line prior to supplying the signal current to the driven circuit," does not remedy the failure of Knapp to describe or suggest the features of amended claim 1 that, as noted above, Knapp fails to describe or suggest.

Accordingly, neither Knapp, Noboru, nor any proper combination of these references describes or suggests a driven circuit including a first transistor and a first precharge circuit electrically connected to a signal line and including a second transistor, where a gate width of the second transistor is larger than a gate width of the first transistor, as recited in amended claim 1.

For at least this reason, applicant requests reconsideration and withdrawal of the rejection of claim 1 and claims 7 and 64, which depend, directly or indirectly, from claim 1.

Claims 18 and 59

Claims 18 and 59 have been rejected as being unpatentable over Knapp in view of Noboru. Applicant requests reconsideration and withdrawal of this rejection because neither Knapp, Noboru, nor any proper combination of these references describes or suggests a driven circuit including a first transistor, a precharge circuit including a second transistor, and a first switch for controlling an electrical connection between the driven circuit and the precharge circuit, where a gate width of the second transistor is larger than a gate width of the first transistor, as recited in amended claim 18.

As discussed above with respect to claim 1, neither Knapp nor Noboru describes or suggests that a gate width of a second transistor is larger than a gate width of a first transistor. Thus, for at least this reason, applicant requests that the rejection of claim 18 be withdrawn.

Additionally, the Office Action acknowledges that Knapp does not disclose a precharge circuit (see Office Action at page 8, lines 5-6), and the Office Action relies on Noboru for this feature asserting that "[i]t would have been obvious at the time of the invention to modify Knapp with the teachings of Noboru, a precharge circuit, because it would improve display characteristics since it would take less time to reach the display voltage because it has been precharged" (see Office Action at page 8, lines 6-10). Applicant respectfully disagrees that it would have been obvious to modify Knapp in the manner suggested by the Office Action.

Noboru relates to a display device. See Noboru at ¶ 0001. In Noboru, electroluminescence devices 10 are arranged in an "mxn" matrix at the intersection of "n" signal lines 11 and "m" scanning lines 12. See Noboru at ¶ 0015. Each signal line 11 is connected to a driving source 15(D) or 17(C) through a signal-line switch 13. See Noboru at ¶ 0015 and Drawing 1. The source 17(C) precharges the signal line to the signal level that emits light from the devices 10. See Noboru at ¶ 0018.

The Office Action appears to equate Noboru's source 17(C) with the recited precharge circuit. See Office Action at page 8, line 6. Additionally, the Office Action equates Knapp's transistor 30 with the recited driven circuit including a first transistor and Knapp's switch 33 with the recited first switch for controlling an electrical connection between the driven circuit and the precharge circuit. See Office Action at page 7, line 21 to 2. Thus, modification of Knapp with Noboru's source 17(C) would result in the source 17(C) being located between

Knapp's switch 33 and the display element 20, or the display element 20 being located between the switch 33 and the source 17(C). However, placing the source 17(C) in either of these locations would not result in the improvement asserted by the examiner. Thus, claim 18 is allowable over Knapp, Noboru, or any proper combination of these references for at least this additional reason.

Accordingly, applicant requests withdrawal of the rejection of claim 18 and claim 59, which depends from claim 18.

Claims 20, 21, 28, 60, 63, and 66

Claims 20, 21, 28, 60, 63, and 66 have been rejected as being unpatentable over Knapp in view of Noboru. Applicant requests reconsideration and withdrawal of this rejection because neither Knapp, Noboru, nor any proper combination of these references describes or suggests a driven circuit including a first transistor, plural precharge circuits, and a first switch for controlling an electrical connection between the driven circuit and the plural precharge circuits, as recited in amended claim 20.

The Office Action acknowledges that neither Knapp nor Noboru describe or suggest plural precharge circuits. See Office Action at page 8, line 17. Thus, Knapp and Noboru also do not describe or suggest a first switch for controlling an electrical connection between a driven circuit and the plural precharge circuits. Moreover, the Office Action provides no basis for why it would have been obvious for one of ordinary skill in the art to bridge the gap between the subject matter of claim 20 and what is disclosed by Knapp and Noboru. See MPEP § 2141 (III), 8th Ed., Rev 6. Rather, the Office Action asserts that "[s]ince there is no benefit or advantage in the specification for having plural precharge circuits, it would have been obvious to one of ordinary skill in the art at the time of the invention to choose either plural precharge circuits or a single precharge circuit based on a designer's choice." See Office Action at page 9, lines 15-18. This is incorrect in that applicant's specification does provide a benefit for having plural precharge circuits. In one non-limiting example from applicant's specification, the description of Figure 17 at page 13, line 31 to page 14, line 10 notes that:

> As described above, the precharge voltage V_p is not always equal to the potential of the node P in a steady state, however, it can be set to the potential close to this one. The magnitude of the

precharge voltage V_p can be set appropriately according to the signal current I. FIG. 17 shows a circuit in which a plurality of precharge voltage V_p is set according to the signal current I and supplied to the node P selectively. For example, the precharge circuit is designed so that a precharge voltage V_{p1} is supplied when the signal current I is 0 to 10mA, a precharge voltage V_{p2} is supplied when the signal current I is 10 to 20 mA, and a precharge voltage V_{p3} is supplied when the signal current I is 20 to 30 mA, then the precharge circuit for supplying these precharge voltages is composed to be connected to terminals A, B, and C. By using a switching circuit 501, S_{W4} to S_{W6} are sequentially switched in accordance with the signal current I for supplying the node P.

An example of a circuit for generating the precharge voltages V_{p1} to V_{p4} using precharge circuits 500A, 500B, 500C, and 500D is shown in Figure 5 and discussed at line 20 of page 22 of the applicant's specification. According to the above example, the circuit shown in Figure 17 may be used to appropriately set the precharge voltage using a plurality of precharge circuits. Thus, the specification discloses a benefit to having multiple precharge circuits; in particular, the multiple precharge circuits permits a particular precharge voltage to be selectively applied to the node P.

Accordingly, Knapp and Noboru, whether taken alone or in combination, fail to describe or suggest a driven circuit including a first transistor, plural precharge circuits, and a first switch for controlling an electrical connection between the driven circuit and the plural precharge circuits, as recited in claim 20. Moreover, the Office Action has not established a basis for concluding that it would have been obvious to one of ordinary skill in the art to bridge the gap between the subject matter of claim 20 and that which is disclosed in Knapp and Noboru.

Applicant requests reconsideration and withdrawal of the rejection of claim 20 and claims 21, 28, 60, 63, and 65, which depend, directly or indirectly, from claim 20.

New Claims

Claims 71-75

New claims 71-75 depend from one of claims 1, 18, and 20 and are believed to be allowable for at least the reasons discussed above with respect to claims 1, 18, and 20.

Claims 76-81

New claim 76 recites, among other features, a driven circuit including a first transistor, a signal line electrically connected to the first transistor through a node, and a first precharge circuit electrically connected to the signal line and including a second transistor, where a gate length of the second transistor is smaller than a gate length of the first transistor. Neither Knapp nor Noboru describe or suggest that a gate length of a second transistor is smaller than a gate length of a first transistor. For at least this reason, claim 76 and claims 77-81, which depend, directly or indirectly, from claim 76, are allowable.

Claims 82-87

New claim 82 recites, among other features, a driven circuit including a first transistor, and a precharge circuit including a second transistor, where a gate length of the second transistor is smaller than a gate length of the first transistor. Neither Knapp nor Noboru describes or suggests that a gate length of a second transistor is smaller than a gate length of a first transistor. For at least this reason, claim 82 and claims 83-87, which depend, directly or indirectly, from claim 82, are allowable.

Conclusion

Applicant submits that all claims are in condition for allowance.

It is believed that all of the pending issues have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this reply should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this reply, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Pursuant to 37 CFR §1.136, Applicants hereby petition that the period for response to the Office Action dated November 1, 2007, be extended for one month to and including March 3, 2008. Applicant notes that March 1, 2008 occurred on a Saturday.

Fees in the amount of $930 for payment of a one-month extension of time fee ($120) and the request for continued examination fee ($810) are being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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